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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,636	11/25/2003	William C. Plants	ACT-280COA	7317

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EXAMINER	
CHANG, ERIC	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/722,636	PLANTS ET AL.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claim 1 is pending.

Drawings

2. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,111,448 to Shibayama in view of U.S. Patent 6,043,677 to Albu, et al.

5. As to claim 1, Shibayama discloses a delay lock loop comprising:

[a] a reference delay line coupled to a reference clock [FIG. 7, element 10, and col. 7, lines 6-22];

[b] a feedback delay line connected to a feedback clock [FIG. 7, element 7, and col. 6, lines 15-17];

[d] a phase detector connected to the divide-by-two circuit and the feedback delay line [FIG. 7, element 8, and col. 6, lines 17-20];

[e] a control circuit coupled to the phase detector [FIG. 7, element 9, and col. 6, lines 20-22];

[f] a programmable delay line connected to the reference clock and the control circuit [FIG. 7, element 6, and col. 6, lines 20-22];

[g] a clock adjuster connected to the programmable delay line [FIG. 13, element 18d, and col. 11, lines 34-47] – although Shibayama teaches a divider circuit as the clock adjuster to reduce the frequency of the distributed signal, it would be obvious to one of ordinary skill in the art to employ a doubler circuit to increase the frequency of the signal, substantially as claimed; and

[h] a clock tree coupled to the clock adjuster and outputting the feedback clock [FIG. 13, element 13, and col. 11, lines 26-33].

Shibayama teaches all of the limitations of the claim but does not teach that a divide-by-two circuit coupled to the reference delay line.

Albu teaches:

[c] a divider circuit coupled to the reference delay line [FIG. 2, element 122];

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ a divider circuit as taught by Albu. One of ordinary skill in the art would have been motivated to do so to manage clock delay and skew [col. 1, lines 12-15].

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of implementing a delayed

lock loop. Moreover, the programmable divider means taught by Albu would improve the flexibility of Shibayama because it allowed the divisor to be programmable, allowing for division by factors other than two [col. 1, lines 51-59]. Furthermore, Albu teaches that the delay lock loop circuit can also be implemented in and for use in FPGA architecture [col. 1, lines 42-59].

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703) 308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ec
June 13, 2004

A. ELAMIN
PRIMARY EXAMINER